



ASint DDR3 Unbuffered SO-DIMM

ASint DDR3 Unbuffered SO-DIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank
x64 Non ECC				
SSZ3128M8-EGN1D	2GB	256M×64	128M×8(ASint 3128M8-GN1D)*16	2
SSZ3128M8-EDJ1D	2GB	256M×64	128M×8(ASint 3128M8-DJ1D)*16	2
SSZ3128M8-EAE1D	2GB	256M×64	128M×8(ASint 3128M8-AE1D)*16	2
SSY3128M8-EGN1D	1GB	128M×64	128M×8(ASint 3128M8-GN1D)*8	1
SSY3128M8-EDJ1D	1GB	128M×64	128M×8(ASint 3128M8-DJ1D)*8	1
SSY3128M8-EAE1D	1GB	128M×64	128M×8(ASint 3128M8-AE1D)*8	1

Grade	Data rate Mbps (max.)	SPEED(CL-tRCD-tRP)	Package	Contact pad
GN	1600	DDR3-1600(11-11-11)	204-pin SO-DIMM (lead-free)	Gold
DJ	1333	DDR3-1333(9-9-9)		
AE	1066	DDR3-1066(7-7-7)		

Specifications

- Density: 1GB&2GB
- Organization
 - 128M words × 64 bits, 1 ranks
 - 256M words × 64 bits, 2 ranks
- Mounting 8/16 pieces of 1G bits DDR3 SDRAM sealed in FBGA
- Package: 204-pin socket type small outline dual in line memory module (SO-DIMM)
 - PCB height: 30.0mm
 - Lead pitch: 0.6mm
 - Lead-free (RoHS compliant) and Halogen-free
- Power supply: VDD = 1.5V ± 0.075V
- Data rate: 1600Mbps/1333Mbps/1066Mbps (max.)
- Eight internal banks for concurrent operation (components)
- Interface: SSTL_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- /CAS Latency (CL): 6, 7, 8, 9, 10, 11
- /CAS write latency (CWL): 5, 6, 7, 8
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
 - Average refresh period
 - 7.8µs at 0°C ≤ TC ≤ +85°C
 - 3.9µs at +85°C < TC ≤ +95°C
- Operating case temperature range
 - TC = 0°C to +95°C

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
 - Synchronous ODT
 - Dynamic ODT
 - Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
 - Normal/extended
- Programmable Output driver impedance control



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Pin Configurations

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREFDQ	103	/CK0	2	VSS	104	/CK1
3	VSS	105	VDD	4	DQ4	106	VDD
5	DQ0	107	A10 (AP)	6	DQ5	108	BA1
7	DQ1	109	BA0	8	VSS	110	/RAS
9	VSS	111	VDD	10	/DQS0	112	VDD
11	DM0	113	/WE	12	DQS0	114	/CS0
13	VSS	115	/CAS	14	VSS	116	ODT0
15	DQ2	117	VDD	16	DQ6	118	VDD
17	DQ3	119	NC	18	DQ7	120	ODT1
19	VSS	121	/CS1	20	VSS	122	NC
21	DQ8	123	VDD	22	DQ12	124	VDD
23	DQ9	125	NC	24	DQ13	126	VREFCA
25	VSS	127	VSS	26	VSS	128	VSS
27	/DQS1	129	DQ32	28	DM1	130	DQ36
29	DQS1	131	DQ33	30	/RESET	132	DQ37
31	VSS	133	VSS	32	VSS	134	VSS
33	DQ10	135	/DQS4	34	DQ14	136	DM4
35	DQ11	137	DQS4	36	DQ15	138	VSS
37	VSS	139	VSS	38	VSS	140	DQ38
39	DQ16	141	DQ34	40	DQ20	142	DQ39
41	DQ17	143	DQ35	42	DQ21	144	VSS
43	VSS	145	VSS	44	VSS	146	DQ44
45	/DQS2	147	DQ40	46	DM2	148	DQ45
47	DQS2	149	DQ41	48	VSS	150	VSS
49	VSS	151	VSS	50	DQ22	152	/DQS5
51	DQ18	153	DM5	52	DQ23	154	DQS5
53	DQ19	155	VSS	54	VSS	156	VSS
55	VSS	157	DQ42	56	DQ28	158	DQ46
57	DQ24	159	DQ43	58	DQ29	160	DQ47
59	DQ25	161	VSS	60	VSS	162	VSS
61	VSS	163	DQ48	62	/DQS3	164	DQ52
63	DM3	165	DQ49	64	DQS3	166	DQ53
65	VSS	167	VSS	66	VSS	168	VSS
67	DQ26	169	/DQS6	68	DQ30	170	DM6
69	DQ27	171	DQS6	70	DQ31	172	VSS
71	VSS	173	VSS	72	VSS	174	DQ54
73	CKE0	175	DQ50	74	CKE1	176	DQ55
75	VDD	177	DQ51	76	VDD	178	VSS
77	NC	179	VSS	78	NC	180	DQ60
79	BA2	181	DQ56	80	NC	182	DQ61
81	VDD	183	DQ57	82	VDD	184	VSS
83	A12	185	VSS	84	A11	186	/DQS7
85	A9	187	DM7	86	A7	188	DQS7
87	VDD	189	VSS	88	VDD	190	VSS
89	A8	191	DQ58	90	A6	192	DQ62
91	A5	193	DQ59	92	A4	194	DQ63
93	VDD	195	VSS	94	VDD	196	VSS
95	A3	197	SA0	96	A2	198	/EVENT
97	A1	199	VDDSPD	98	A0	200	SDA
99	VDD	201	SA1	100	VDD	202	SCL
101	CK0	203	VTT	102	CK1	204	VTT

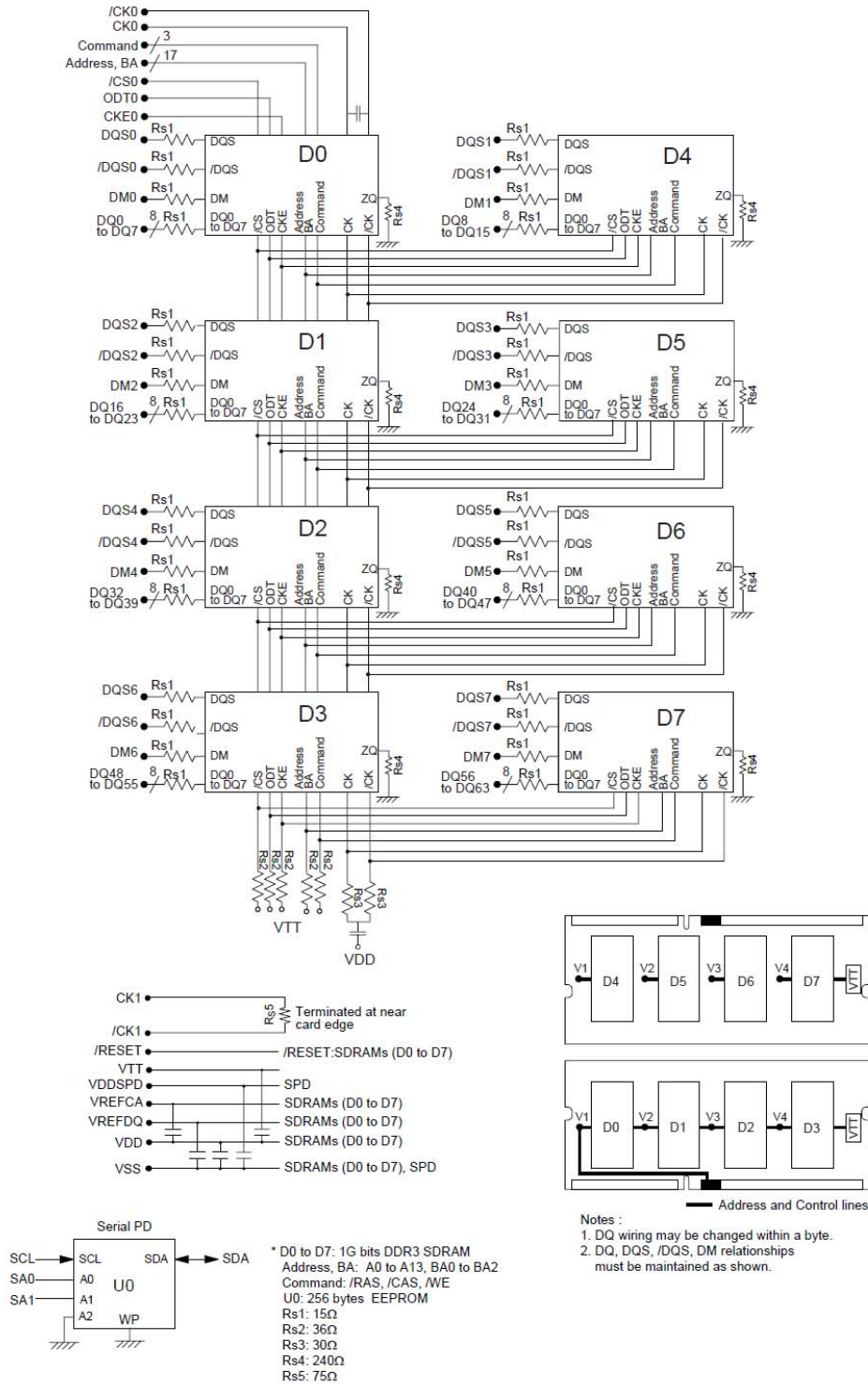


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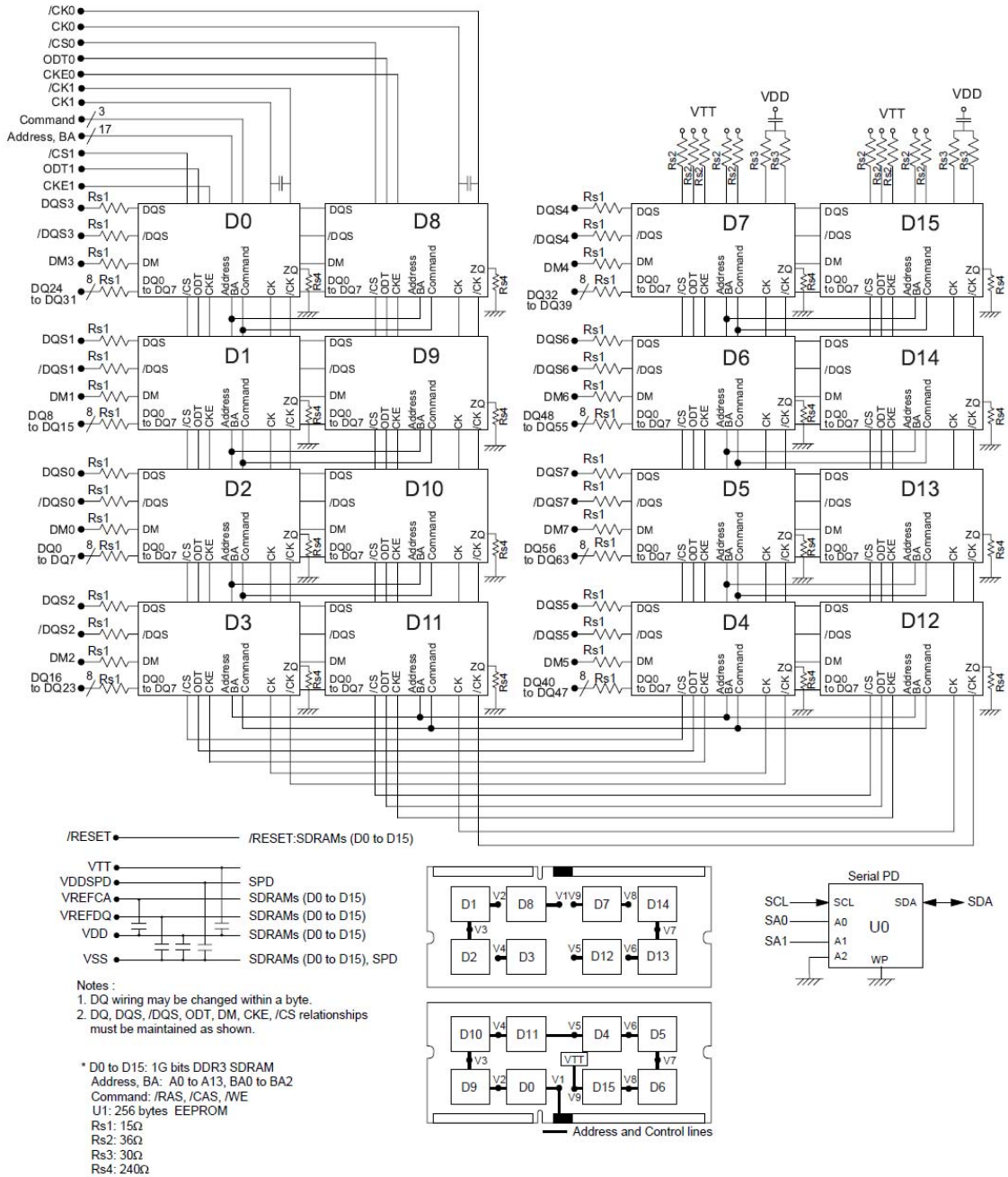
Pin Description

Pin name	Function
A0 to A13 A10 (AP) A12 (/BC)	Address input Row address A0 to A13 Column address A0 to A9 Auto precharge Burst Chop
BA0, BA1,BA2	Bank select address
DQ0 to DQ63	Data input/output
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0,/CS1(for 2 rank)	Chip select
CKE0,CKE1(for 2 rank)	Clock enable
CK0, CK1	Clock input
/CK0, /CK1	Differential clock input
DQS0 to DQS7, /DQS0 to /DQS7	Input and output data strobe
DM0 to DM7	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0, SA1, SA2	Serial address input
VDD	Power for internal circuit
VDDSPD	Power for serial EEPROM
VREFCA	Reference voltage for CA
VREFDQ	Reference voltage for DQ
VTT	I/O termination supply for SDRAM
VSS	Ground
ODT0,ODT1(for 2 rank)	ODT control
NC	No connection

Block Diagram (1 Rank)



Block Diagram (2 Rank)



Electrical Specifications

• All voltages are referenced to VSS (GND).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Power supply voltage	VDD	-0.4 to +1.975	V	1,3,4
Input voltage	VIN	-0.4 to +1.975	V	1,4
Output voltage	VOOUT	-0.4 to +1.975	V	1,4
Reference voltage	VREFCA	-0.4 to 0.6 × VDD	V	3,4
Reference voltage for DQ	VREFDQ	-0.4 to 0.6 × VDDQ	V	3,4
Storage temperature	Tstg	-55 to +100	°C	1,2,4
Power dissipation	PD	8	W	
Short circuit output current	IOOUT	50	mA	1,4

Notes:

- Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage temperature is the case surface temperature on the center/top side of the DRAM.
- VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
- DDR3 SDRAM component specification.

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1,2,3

Notes:

- Operating temperature is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)
 - If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).



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Recommended DC Operating Conditions (TC = 0°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply voltage	VDD, VDDQ	1.425	1.5	1.575	V	1,2,3
	VSS	0	0	0	V	1
	VDDSPD	3.0	3.3	3.6	V	
Input reference voltage	VREFCA (DC)	$0.49 \times VDDQ$	$0.50 \times VDDQ$	$0.51 \times VDDQ$	V	1,4,5
Input reference voltage for DQ	VREFDQ (DC)	$0.49 \times VDDQ$	$0.50 \times VDDQ$	$0.51 \times VDDQ$	V	1,4,5
Termination voltage	VTT	$VDDQ/2 - TBD$	TBD	$VDDQ/2 + TBD$	V	

Notes:

1. DDR3 SDRAM component specification.
2. Under all conditions VDDQ must be less than or equal to VDD.
3. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
4. The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than $\pm 1\%$ VDD (for reference: approx ± 15 mV).
5. For reference: approx. $VDD/2 \pm 15$ mV.



ASint DDR3 Unbuffered SO-DIMM

DC Characteristics 1 (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V, VSS = 0V)

Parameter	Symbol	Data rate (Mbps)	max.	Unit	Notes
Operating current (ACT-PRE) (Another rank is in IDD2P1)	IDD0	1600	1200	mA	
		1333	1080		
		1066	960		
Operating current (ACT-PRE) (Another rank is in IDD3N)	IDD0	1600	1440	mA	
		1333	1280		
		1066	1160		
Operating current (ACT-READ-PRE) (Another rank is in IDD2P1)	IDD1	1600	1320	mA	
		1333	1200		
		1066	1080		
Operating current (ACT-READ-PRE) (Another rank is in IDD3N)	IDD1	1600	1560	mA	
		1333	1400		
		1066	1280		
Precharge power-down standby current	IDD2P1	1600	720	mA	Fast PD Exit
		1333	640		
		1066	560		
	IDD2P0	1600	240	mA	Slow PD Exit
		1333	224		
		1066	208		
Precharge standby current	IDD2N	1600	1040	mA	
		1333	960		
		1066	880		
Precharge standby ODT current	IDD2NT	1600	1040	mA	
		1333	960		
		1066	880		
Precharge quiet standby current	IDD2Q	1600	960	mA	
		1333	880		
		1066	800		
Active power-down current (Always fast exit)	IDD3P	1600	720	mA	
		1333	640		
		1066	560		
Active standby current	IDD3N	1600	1200	mA	
		1333	1040		
		1066	960		
Operating current (Burst read operating) (Another rank is in IDD2P1)	IDD4R	1600	2200	mA	
		1333	1920		
		1066	1560		
Operating current (Burst read operating) (Another rank is in IDD3N)	IDD4R	1600	2440	mA	
		1333	2120		
		1066	1760		
Operating current (Burst write operating) (Another rank is in IDD2P1)	IDD4W	1600	2280	mA	
		1333	2000		
		1066	1640		
Operating current (Burst write operating) (Another rank is in IDD3N)	IDD4W	1600	2520	mA	
		1333	2200		
		1066	1840		
Burst refresh current (Another rank is in IDD2P1)	IDD5B	1600	2600	mA	
		1333	2480		
		1066	2360		
Burst refresh current (Another rank is in IDD3N)	IDD5B	1600	2840	mA	
		1333	2680		
		1066	2560		
All bank interleave read current (Another rank is in IDD2P1)	IDD7	1600	3160	mA	
		1333	2800		
		1066	2440		
All bank interleave read current (Another rank is in IDD3N)	IDD7	1600	3400	mA	
		1333	3000		
		1066	2640		

Self-Refresh Current (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V)

Parameter	Symbol	Max.	Unit	Notes
Self-refresh current normal temperature range	IDD6	160	mA	
Self-refresh current extended temperature range	IDD6ET	288	mA	
Auto self-refresh current (optional)	IDD6TC	-	mA	

Timings used for IDD and IDDQ Measurement-Loop Patterns

Parameter	DDR3-1600	DDR3-1333	DDR3-1066	Unit
	11-11-11	9-9-9	7-7-7	
CL	11	9	7	tCK
tCK min.	1.25	1.5	1.875	ns
nRCD min.	11	9	7	nCK
nRC min.	39	33	27	nCK
nRAS min.	28	24	20	nCK
nRP min.	11	9	7	nCK
nFAW	24	20	20	nCK
nRRD	5	4	4	nCK
nRFC	88	74	59	nCK

**DC Characteristics 2 (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)
(DDR3 SDRAM Component Specification)**

Parameter	Symbol	Value	Unit	Notes
Input leakage current	ILI	2	μA	VDD ≥ VIN ≥ VSS
Output leakage current	ILO	5	μA	DDQ ≥ VOUT ≥ VSS

Pin Functions

Symbol	Type	Function																																				
CK, /CK	Input	CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).																																				
/CS	Input	All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.																																				
/RAS, /CAS, /WE	Input	/RAS, /CAS and /WE (along with /CS) define the command being entered.																																				
A0 to A13	Input	<p>Provided the row address for active commands and the column address for read/write commands to select one location out of the memory array in the respective bank. (A10(AP) and A12(/BC) have additional functions, see below) The address inputs also provide the op-code during mode register set commands.</p> <p>[Address Pins Table]</p> <table border="1"> <tr> <td>Address (A0 to A13)</td> <td></td> </tr> <tr> <td>Row address (RA)</td> <td>Column address (CA)</td> </tr> <tr> <td>AX0 to AX13</td> <td>AY0 to AY9</td> </tr> </table>	Address (A0 to A13)		Row address (RA)	Column address (CA)	AX0 to AX13	AY0 to AY9																														
Address (A0 to A13)																																						
Row address (RA)	Column address (CA)																																					
AX0 to AX13	AY0 to AY9																																					
A10 (AP)	Input	<p>A10 is sampled during read/write commands to determine whether auto-precharge should be performed to the accessed bank after the read/write operation. (high: auto-precharge; low: no auto-precharge)</p> <p>A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = low) or all banks (A10 = high). If only one bank is to be precharged, the bank is selected by bank addresses (BA).</p>																																				
A12(/BC)	Input	<p>A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed.</p> <p>(A12 = high: no burst chop, A12 = low: burst chopped.)</p>																																				
BA0, BA1, BA2	Input	<p>BA0, BA1 and BA2 define to which bank an active, read, write or precharge command is being applied. BA0 and BA1 also determine if a mode register is to be accessed during a MRS cycle.</p> <p>[Bank Select Signal Table]</p> <table border="1"> <thead> <tr> <th></th> <th>BA0</th> <th>BA1</th> <th>BA2</th> </tr> </thead> <tbody> <tr> <td>Bank 0</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>Bank 1</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>Bank 2</td> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>Bank 3</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>Bank 4</td> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>Bank 5</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>Bank 6</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>Bank 7</td> <td>H</td> <td>H</td> <td>H</td> </tr> </tbody> </table> <p>Remark: H: VIH. L: VIL.</p>		BA0	BA1	BA2	Bank 0	L	L	L	Bank 1	H	L	L	Bank 2	L	H	L	Bank 3	H	H	L	Bank 4	L	L	H	Bank 5	H	L	H	Bank 6	L	H	H	Bank 7	H	H	H
	BA0	BA1	BA2																																			
Bank 0	L	L	L																																			
Bank 1	H	L	L																																			
Bank 2	L	H	L																																			
Bank 3	H	H	L																																			
Bank 4	L	L	H																																			
Bank 5	H	L	H																																			
Bank 6	L	H	H																																			
Bank 7	H	H	H																																			
CKE	Input	<p>CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self-refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.</p>																																				
DQ	In/Out	Bi-directional data bus.																																				
DQS and /DQS	In/Out	Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signals /DQS to provide differential pair signaling to the system during READs and WRITEs.																																				
ODT	Input	ODT (registered high) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS, DM. The ODT pin will be ignored if the mode register (MR1) is programmed to disable ODT.																																				
DM	Input	DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and /DQS.																																				
VDD	Supply	1.5V is applied. (VDD is for the internal circuit.)																																				
VDDSPD	Supply	3.3V is applied (For serial EEPROM).																																				



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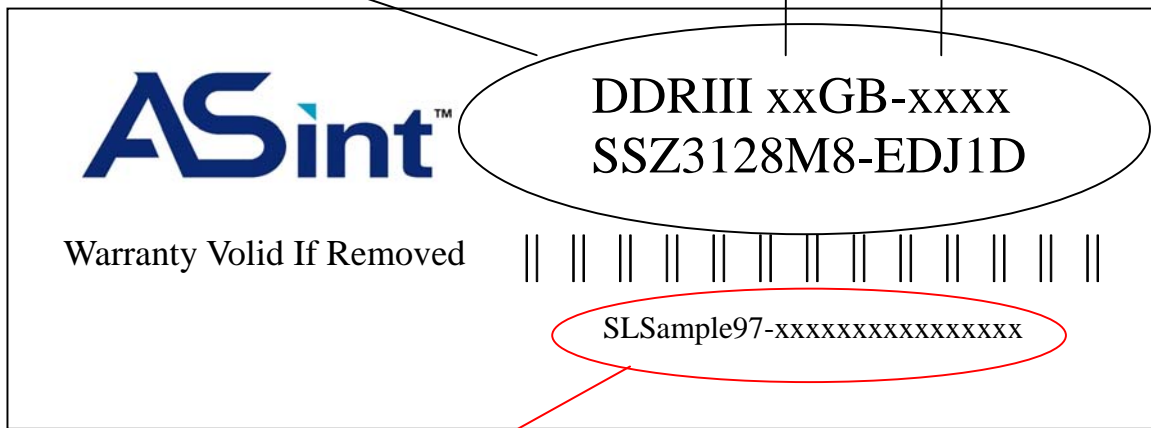
Symbol	Type	Function
VSS	Supply	Ground is connected.
VTT	Supply	I/O termination supply for SDRAM.
VREFDQ	Supply	Reference voltage for DQ.
VREFCA	Supply	Reference voltage for CA.
/RESET	Input	/RESET is negative active signal (active low) and is referred to GND.

Part number decoder for Module

The serial number is fix ;
It's Module ID No. .

Capacity

Speed



The serial number is randomly changeable ;
Please don't care about it.



ASint DDR3 Unbuffered SO-DIMM

Revision History

Revision 0.1 (Aug. 5th 2009)

- Initial Release for ASint DDR3 Unbuffered SO-DIMM